

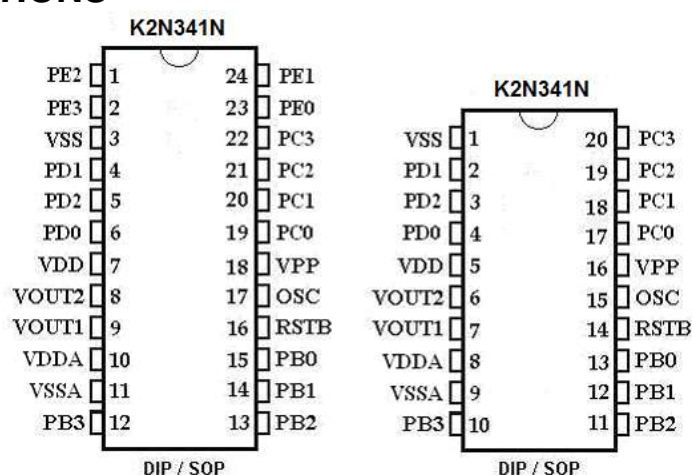


## CPU Addressing Trigger with BUSY and /BUSY Outputs

### FEATURES

- Addressing Mode Trigger
- BUSY and complementary /BUSY outputs
- Up to 128 voice groups
- Any combination of the trigger options:  
    Level/Edge; Hold/Un-hold; Retrigger/Non-retrigger
- DAC through VOUT2\_COUT pin
- PWM through VOUT1 and VOUT2
- No signal output supported
- Support 8-bit PCM, 5-bit uLaw and 4-bit ADPCM compression

### PIN CONFIGURATIONS



### PIN DESCRIPTIONS

Pin Names	Description
VOUT1	PWM output to drive speaker directly
VOUT2_COUT	PWM output or COUT DAC output select by programmable option
VSS/VSSA	Power Ground / Analog Power Ground
OSC	Oscillator input
VPP	Program power pin, leave during playback
VDD/VDDA	Positive Power Supply / Analog Positive Power Supply
PB0	TG Input pin with internal pull-down
PB1, PB2, PB3	Address input pins with internal pull-down
PC0, PC1, PC2, PC3	Address input pins with internal pull-down
PD0	Unused I/O pins, leave open
PD1	BUSY output, active HIGH during voice playback
PD2	/BUSY output, active LOW during voice playback
PE0, PE1, PE2, PE3	Unused I/O pins, leave open
RSTB	Reset pin, Low active

Pins for programming are: VDD, VDDA, VPP, VSS, VSSA, PB0, PB1, OSC, VOUT2 and RSTB.



## Ramp-up-down enable or disable

When COUT is used for playback, Ramp-up-down would be enabled. This function eliminates the 'POP' noise at the beginning and end of voice playback.

When VOUT1 and VOUT2 are used to drive speaker directly, the Ramp-up-down operation are disabled.

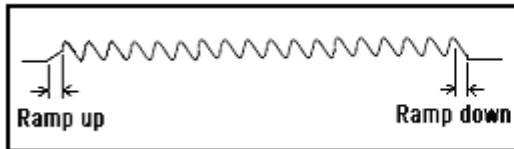


Fig. 1 Ramp-up-down Enable

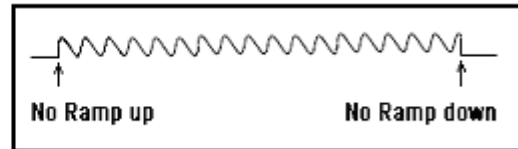


Fig.2 Ramp-up-down Disable

## CPU Addressing Trigger Mode

In this mode, PB1, PB2, PB3, PC0 to PC3 are set to HIGH or LOW to provide the Group address for which the Group to be played. It is then followed by setting the PB0 input pin to HIGH, to strobe the Group address into the chip to start the actual playback.

PB1 = ADDR0 (least signification bit)

PB2 = ADDR1

PB3 = ADDR2

PC0 = ADDR3

PC1 = ADDR4

PC2 = ADDR5

PC3 = ADDR6 (most signification bit)

e.g. [ADDR6:ADDR0] = 0000000 => play Group #1

e.g. [ADDR6:ADDR0] = 0000100 => play Group #4

e.g. [ADDR6:ADDR0] = 1111111 => play Group #128

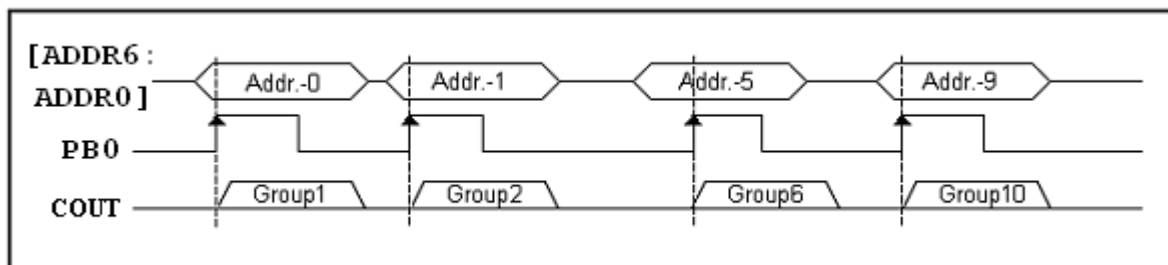


Fig. 3 CPU Address Trigger Mode



## Trigger Options

User selectable options that affect each individual group are called Group Options. They are:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or non-retriggerable

Fig. 4 to Fig. 5 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

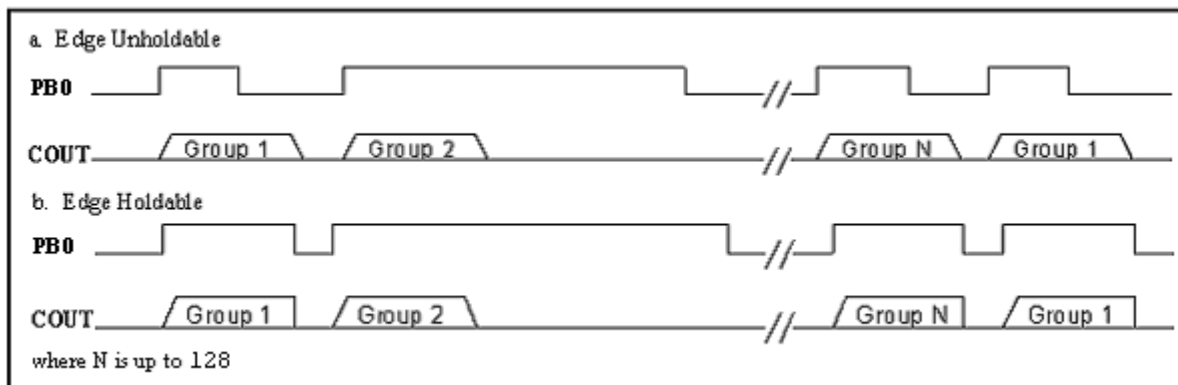


Fig. 4 Trigger with Edge Holdable and Unholdable option

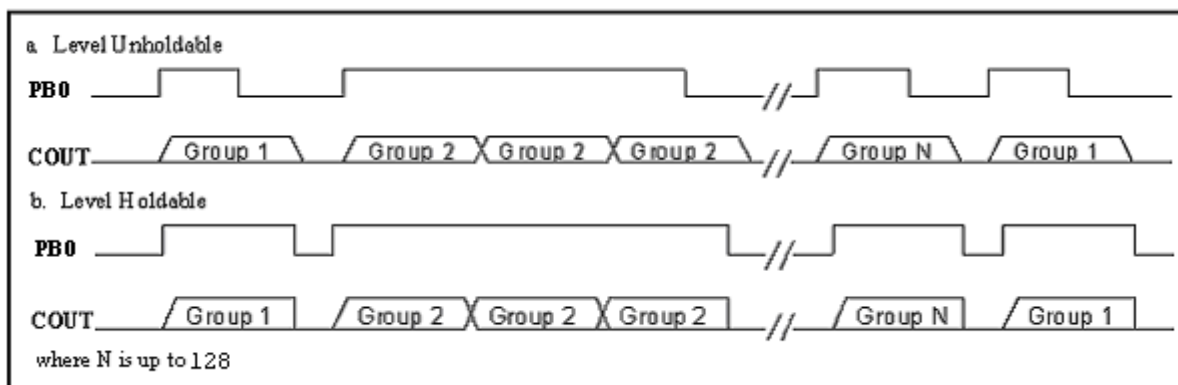
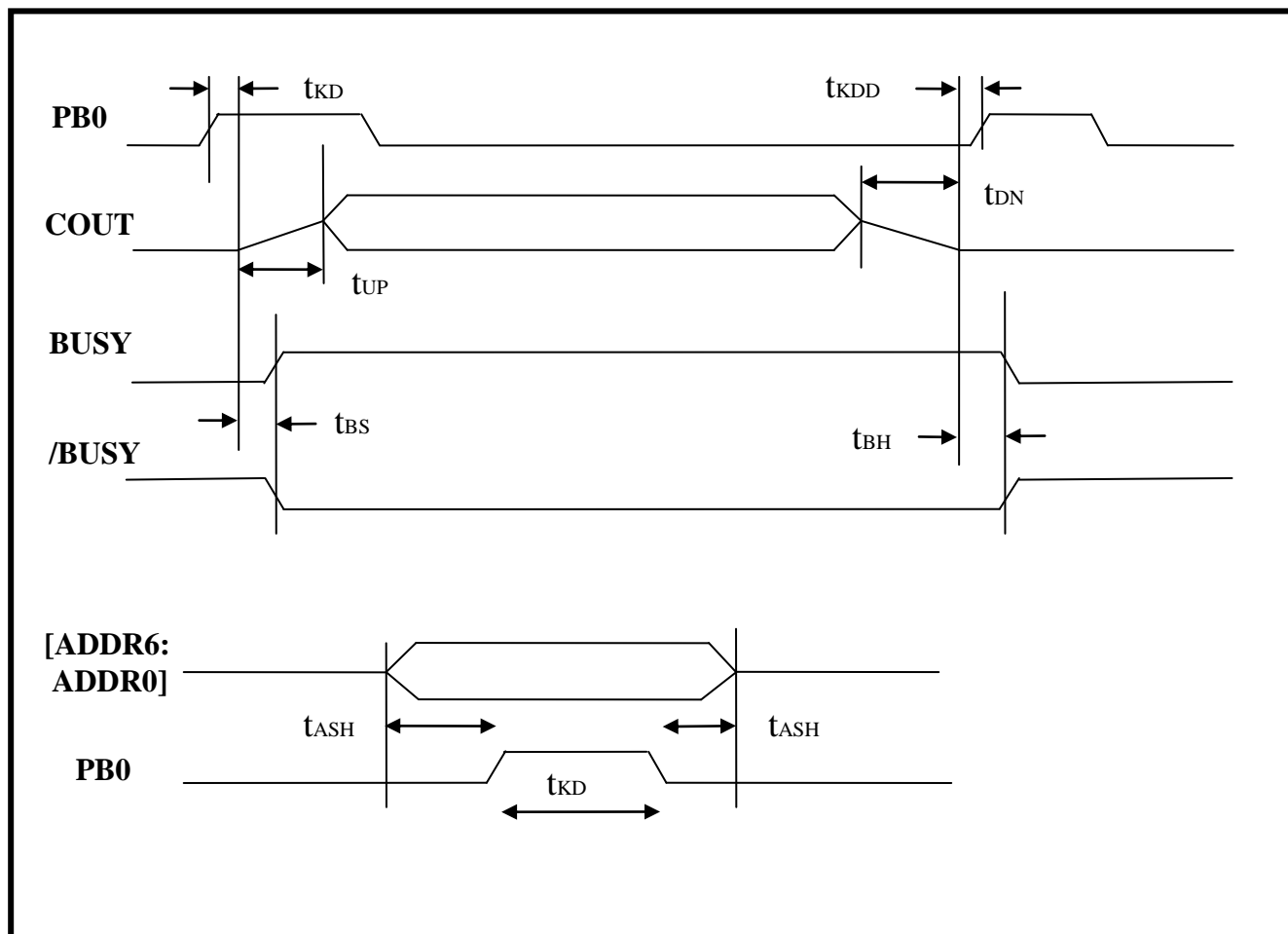


Fig. 5 Trigger with Level Holdable and Unholdable option



## TRIGGER TIMING



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
$t_{KD}$	Key trigger debounce time	20	—	—	ms	1
$t_{WK}$	Wake up time	0	100	200	ms	1
$t_{KDD}$	Key trigger delay after ramp down	--	0	--	ms	
$t_{UP}$	Ramp up time	0		40	ms	1
$t_{DN}$	Ramp down time	0	--	80	ms	2
$t_{BS}$	BUSY output set up time	0	--	1	ms	1
$t_{BH}$	BUSY output set hold time	0	--	1	ms	1
$t_{ASH}$	Address set-up / hold time	1	—	—	ms	1

Note:

- 1) If IC is in standby status, it needs to wait  $t_{WK}$  time, then it starts re-working.
- 2) Ramp down from the value of the last sound sample. Max. time means ramp down from Voice data equal to FF(hex).

# TYPICAL APPLICATIONS

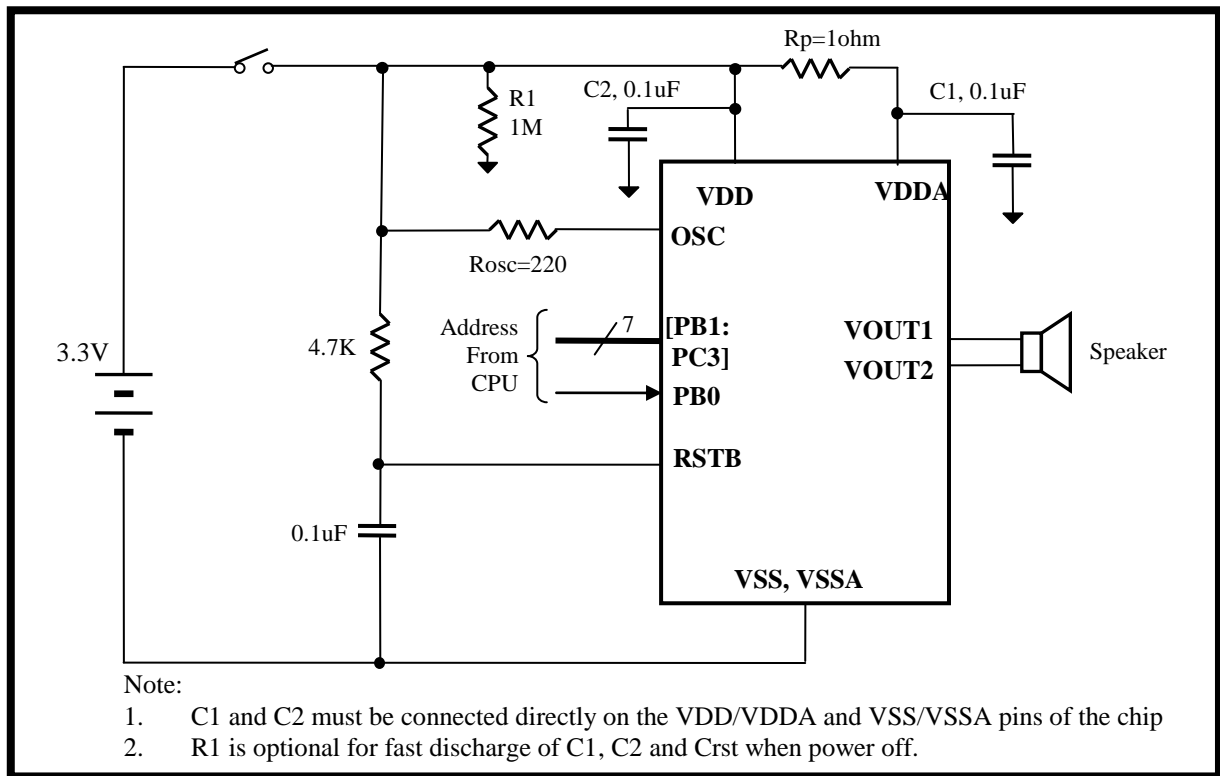


Fig 6. 3.3V Battery with PWM speaker direct drive

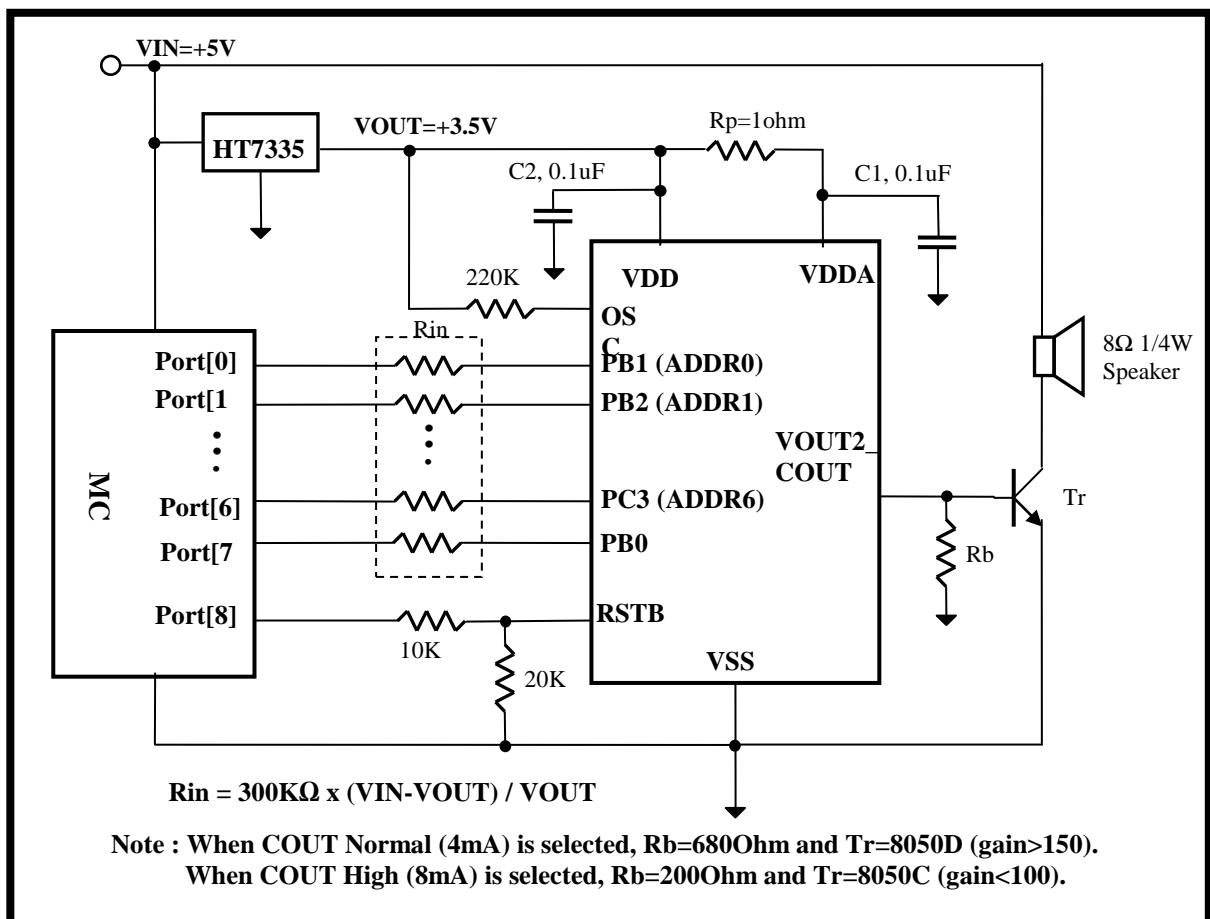


Fig 7. 5V Battery with Transistor direct drive



## Bonding Diagrams



Note: Substrate must be connected to VSS