K2N341 – 341 sec

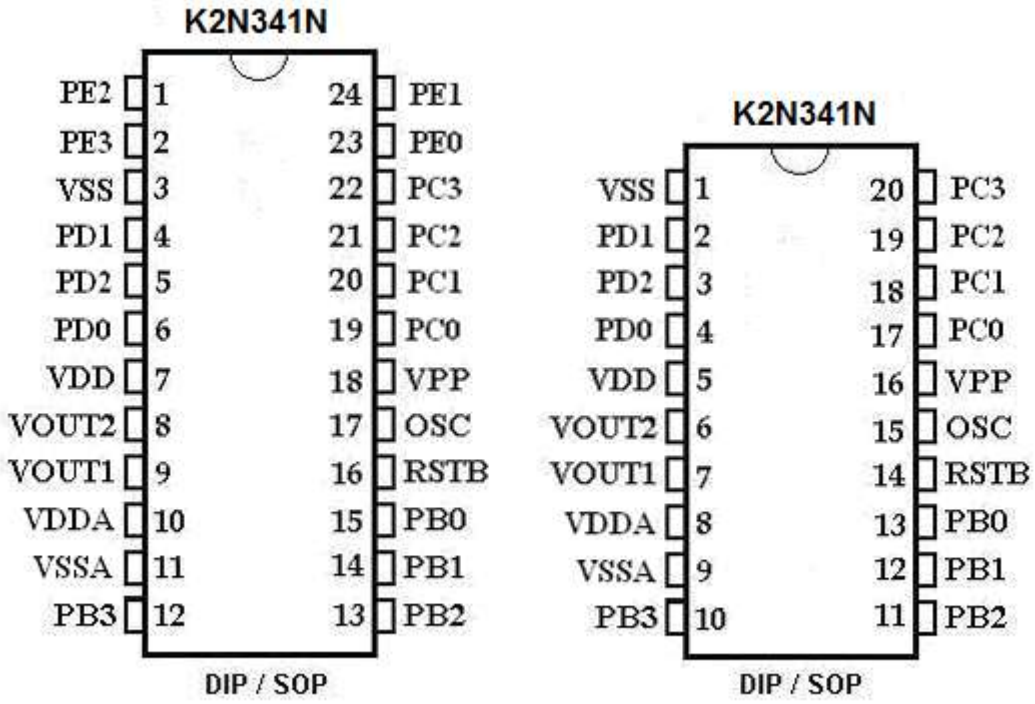
DESCRIPTION

K2N341N is a 8-bit MCU based Voice chip. It is manufactured with Standard CMOS process with embedded voice storage memory. It can store 341sec voice message with 4-bit ADPCM compression at 6KHz sampling rate. 8-bit PCM is also available as user selectable option to improve sound quality. There are up to fifteen programmable I/O pins. Key trigger and Parallel CPU trigger mode can be configured according to different application requirement. User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 9-bit resolution current mode D/A output and PWM direct speaker driving minimize the number of external components. Volume control for both DAC and VOUT output is available.

FEATURES

- Standard CMOS process.
- Embedded EPROM.
- Embedded 8-bit MCU.
- 341sec voice duration at 6 KHz sampling with 4-bit ADPCM compression.
- Combination of voice building blocks to extend playback duration.
- Table entries are available for voice block combinations.
- User selectable PCM or ADPCM data compress.
- Voice Group Trigger Options: Edge / Level; Hold / Un-hold; Retrigger / Non-retrigger.
- Programmable I/Os, Timer Interrupt and Watch Dog Timer.
- Built-in oscillator with fixed Rosc, software control sampling frequency
- 2.4V – 3.6V single power supply and < 5uA low stand-by current.
- PWM Vout1 and Vout2 drive speaker directly.
- D/A COUT with ramp-up ramp-down option to drive speaker through an external BJT.
- Volume control.
- Maximum 9-bit resolution.
- Internal Power-up reset circuit built-in; RSTB provides external control reset to the chip.

PIN CONFIGURATION



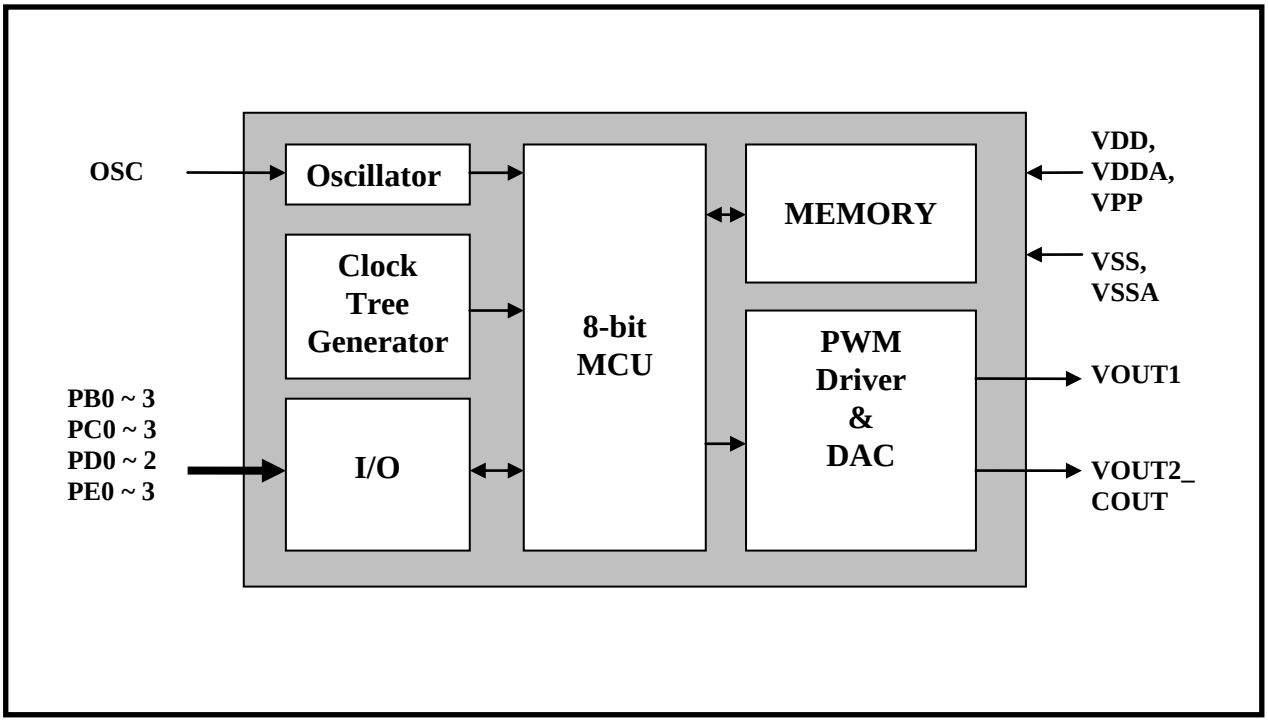
PIN DESCRIPTIONS

Pin Names	Description
VOUT1	PWM output to drive speaker directly
VOUT2_COUT	PWM output or COUT DAC output select by programmable option
VSS	Power Ground
VSSA	Analog Power Ground
OSC	Oscillator input
VDD	Positive Power Supply
VDDA	Analog Positive Power Supply
VPP	Positive Power for EPROM programming, NC during voice playback
PB0~PB3	Programmable I/O port B
PC0~PC3	Programmable I/O port C
PD0~PD2	Programmable I/O port D
PE0~PE3	Programmable I/O port E
RSTB	Reset pin, Low active;

Note:

- PB, PC, PD and PE ports are software programmable I/O pins that can be set to different configurations such as pure input, input with pull-up, input with pull-down and output. The programmable I/O pins set up will take effect immediately after chip RESET is applied.
- Pins for memory programming are: VDD, VDDA, VSS, VSSA, VPP, PB0, PB1, OSC, VOUT2 and RSTB.

BLOCK DIAGRAM



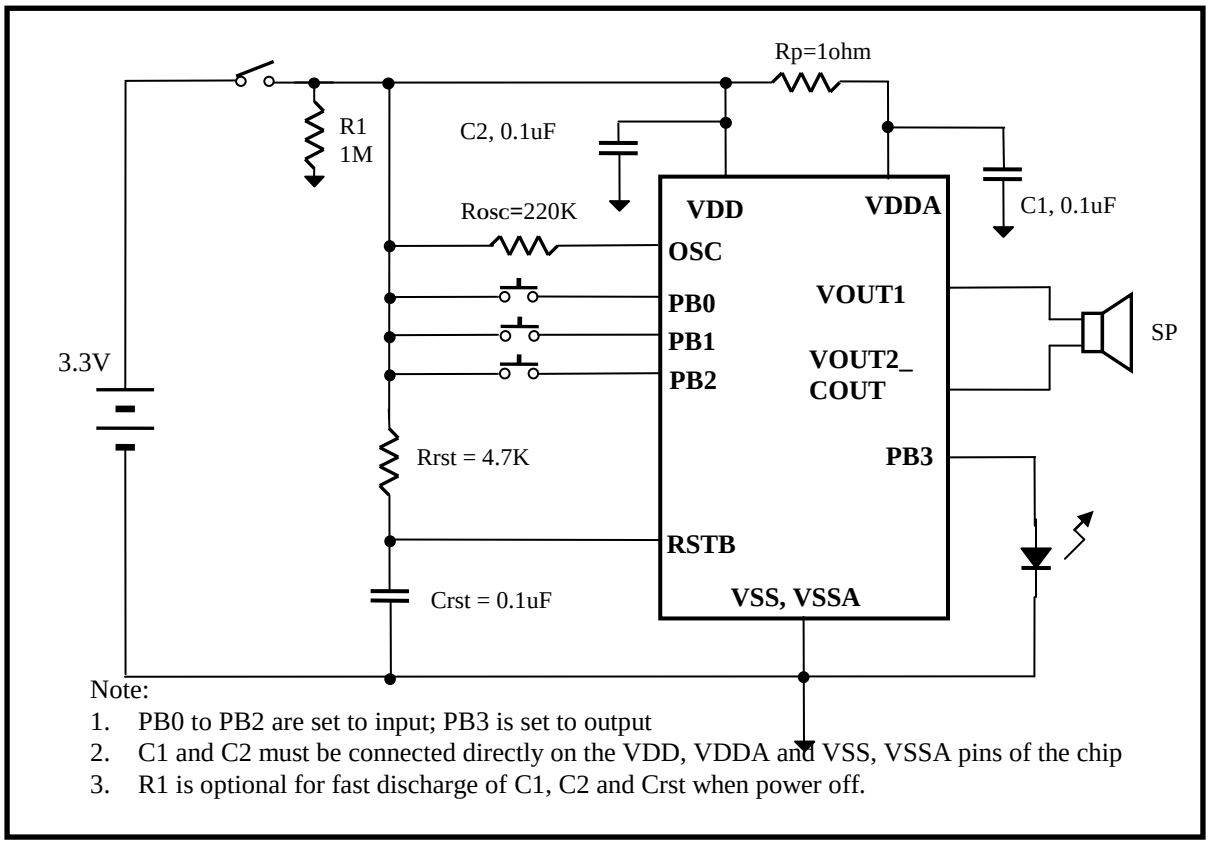
ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +4.0	V
V_{IN}	V_{SS} - 0.3<V_{IN}<V_{DD} + 0.3	V
V_{OUT}	V_{SS} <V_{OUT}<V_{DD}	V
T (Operating):	0 ~ +85	℃
T (Junction)	-40 ~ +125	℃
T (Storage)	-55 ~ +125	℃

DC CHARACTERISTICS (T_A = 0 to 70℃, V_{DD} = 3.0V, V_{SS} = 0V)

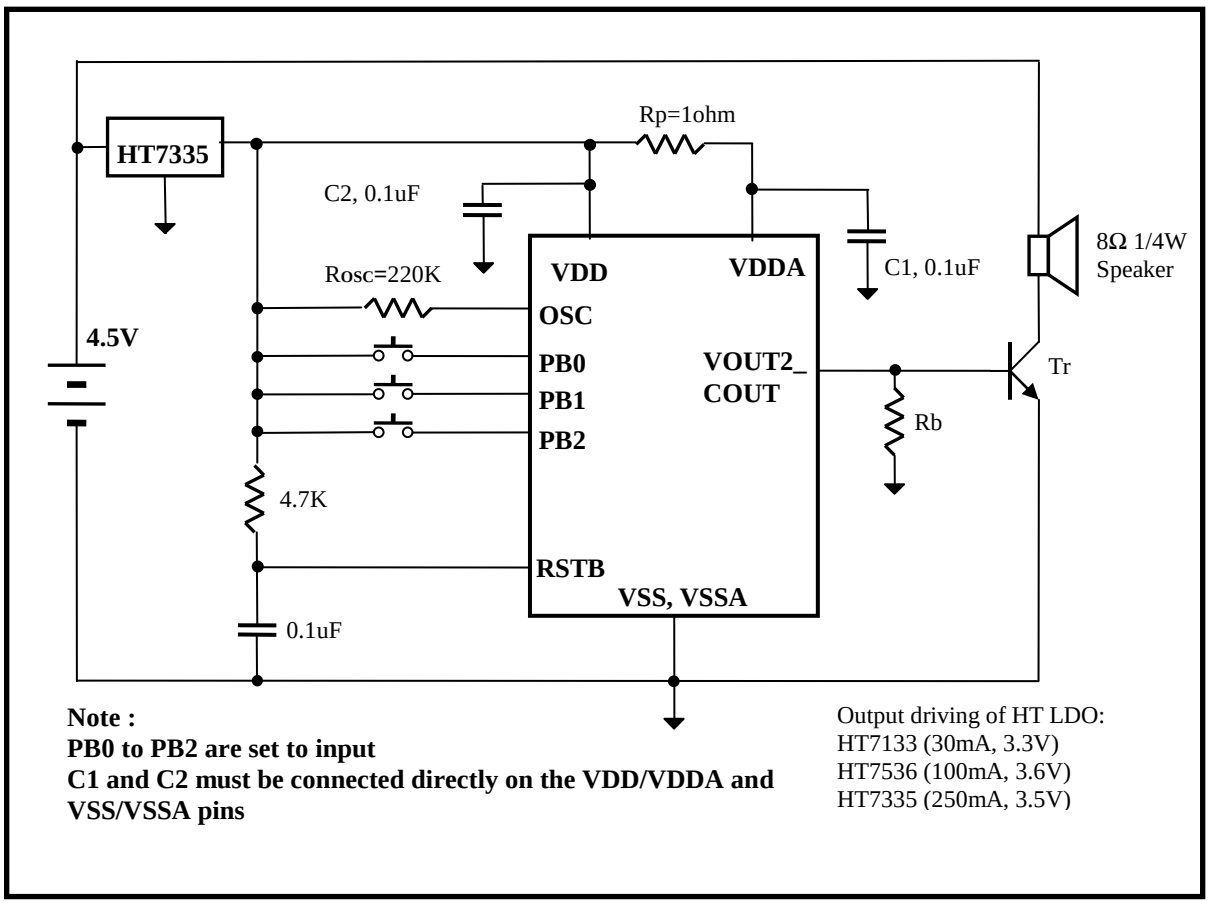
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	2.2	3.0	3.6	V	
I_{SB}	Standby current	—	1	5	μA	I/O properly terminated
I_{OP}	Operating current	—	7	—	mA	I/O properly terminated
V_{IH}	"H" Input Voltage	2.5	3.0	3.5	V	V_{DD}=3.0V
V_{IL}	"L" Input Voltage	-0.3	0	0.5	V	V_{DD}=3.0V
I_{VOUTL_N}	V_{OUT} low O/P Current (Normal Volume)	—	130	—	mA	Vout=1.0V
I_{VOUTL_H}	V_{OUT} low O/P Current (High Volume)	—	200	—	mA	Vout=1.0V
I_{VOUTH_N}	V_{OUT} high O/P Current (Normal Volume)	—	-130	—	mA	Vout=2.0V
I_{VOUTH_H}	V_{OUT} high O/P Current (High Volume)	—	-200	—	mA	Vout=2.0V
I_{CO}	C_{OUT} O/P Current	—	-2	—	mA	Data = 80h
I_{OH}	O/P High Current	—	-10	—	mA	V_{OH}=2.5V
I_{OL}	O/P Low Current	—	17	—	mA	V_{OL}=0.3V
RN_{VOUT}	VOUT pull-down resistance	—	100K	—	**Ω**	VOUT pin set to internal pull-down
RN_{PIO}	Programmable IO pin pull-down resistance	—	1M	—	**Ω**	PBx, PCx, PDx set to internal pull-down
RU_{PIO}	Programmable IO pin pull-up resistance	3.3K	4.7K	—	**Ω**	PBx, PCx, PDx set to internal pull-up
ΔFs/Fs	Frequency stability	-3	—	+3	%	V_{DD} = 3V +/- 0.4V
ΔFc/Fc	Chip to chip Frequency Variation	-5	—	+5	%	Also apply to lot to lot variation

TYPICAL APPLICATIONS



Note:
1. PB0 to PB2 are set to input; PB3 is set to output
2. C1 and C2 must be connected directly on the VDD, VDDA and VSS, VSSA pins of the chip
3. R1 is optional for fast discharge of C1, C2 and Crst when power off.

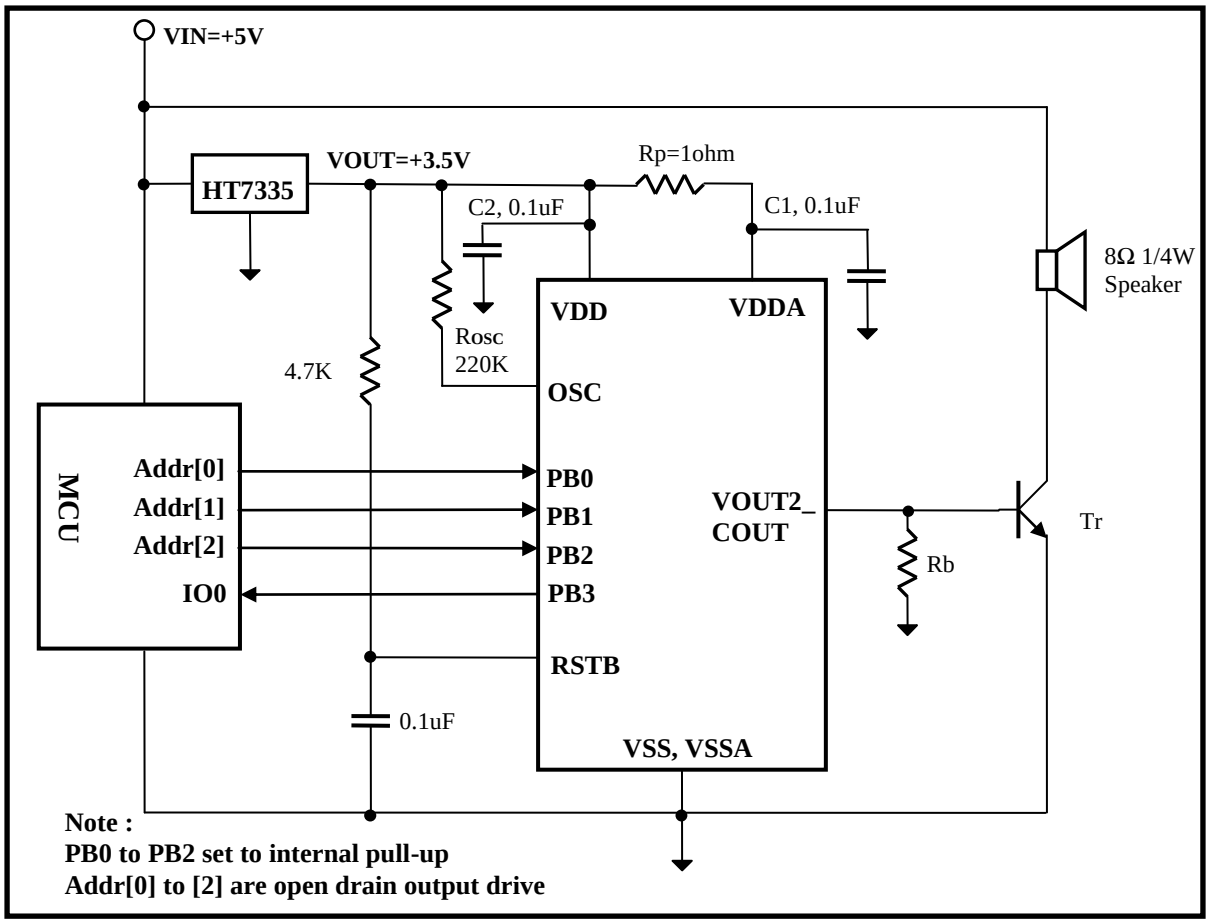
Using 3.3V Battery Direct Drive Speaker



Note :
PB0 to PB2 are set to input
C1 and C2 must be connected directly on the VDD/VDDA and VSS/VSSA pins

Output driving of HT LDO:
HT7133 (30mA, 3.3V)
HT7536 (100mA, 3.6V)
HT7335 (250mA, 3.5V)

Using 4.5V Battery with COUT speaker drive

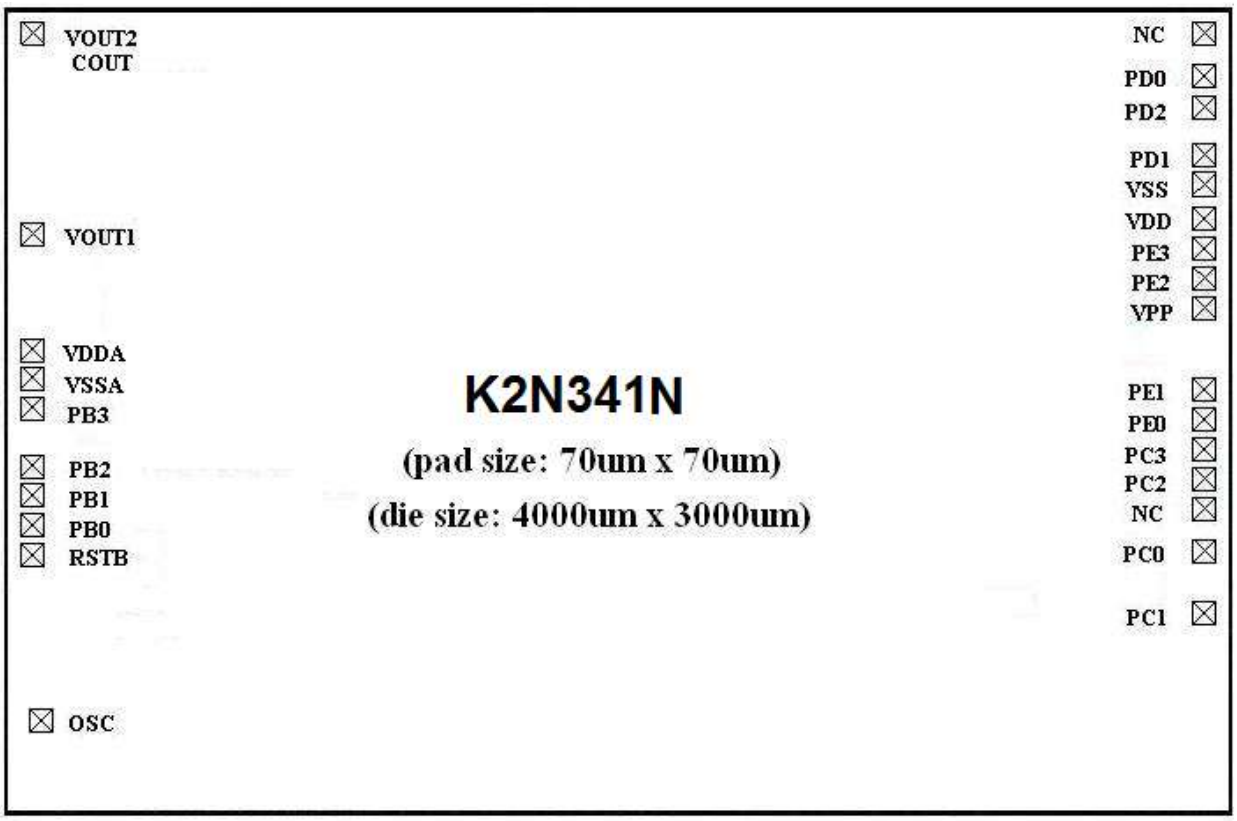


5V CPU Control with COUT

Note for COUT speaker drive:

1. C1 and C2 must be connected as close to the VDD/VDDA and VSS/VSSA pins as possible.
2. Rb is base resistor from 120 Ohm to 390 Ohm depends on value of VDD and transistor gain.
3. Tr is an NPN transistor with beta larger than 150, e.g. 8050D.
4. Rosc = 220K Ohm with Vdd=3.0V can support sampling rate up to 14KHz.

Bonding Diagrams



Note: Substrate must be connected to VSS